

METHOD AND SYSTEM FOR DESKEWING
PARALLEL BUS CHANNELS TO INCREASE
DATA TRANSFER RATES

Inventors: Ejaz Ul Haq, et al.
Serial No.: 10/086,594

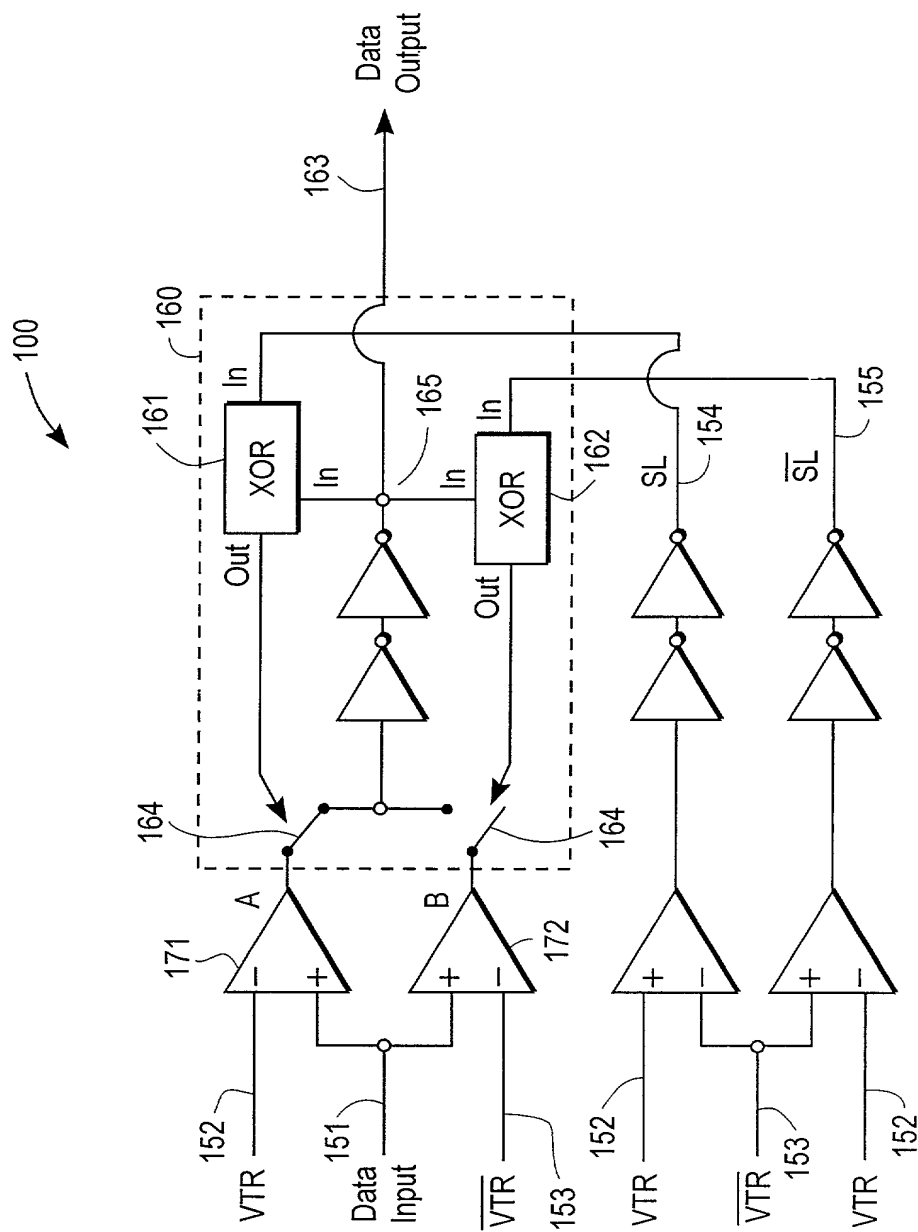


FIG. 1A

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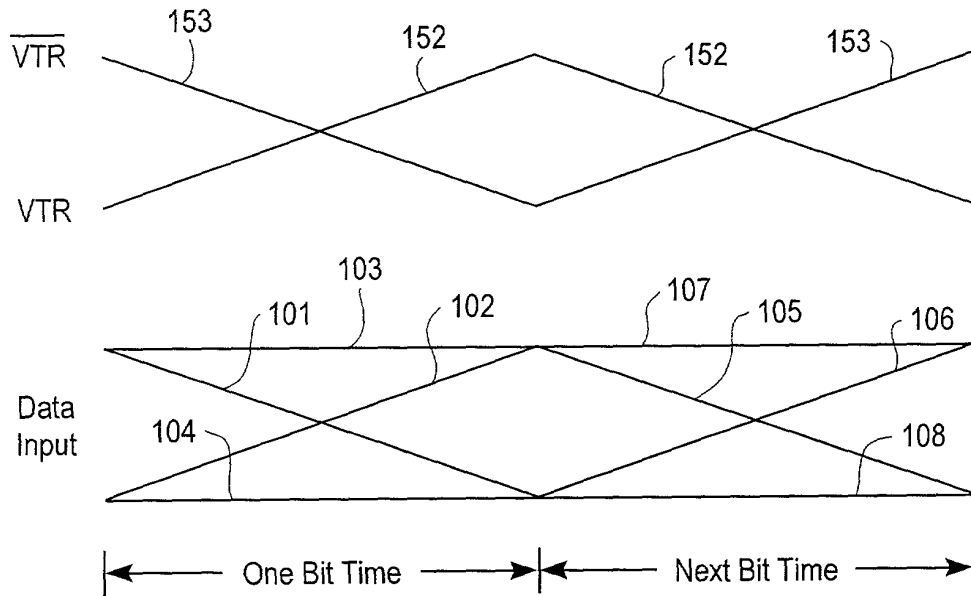


FIG. 1B

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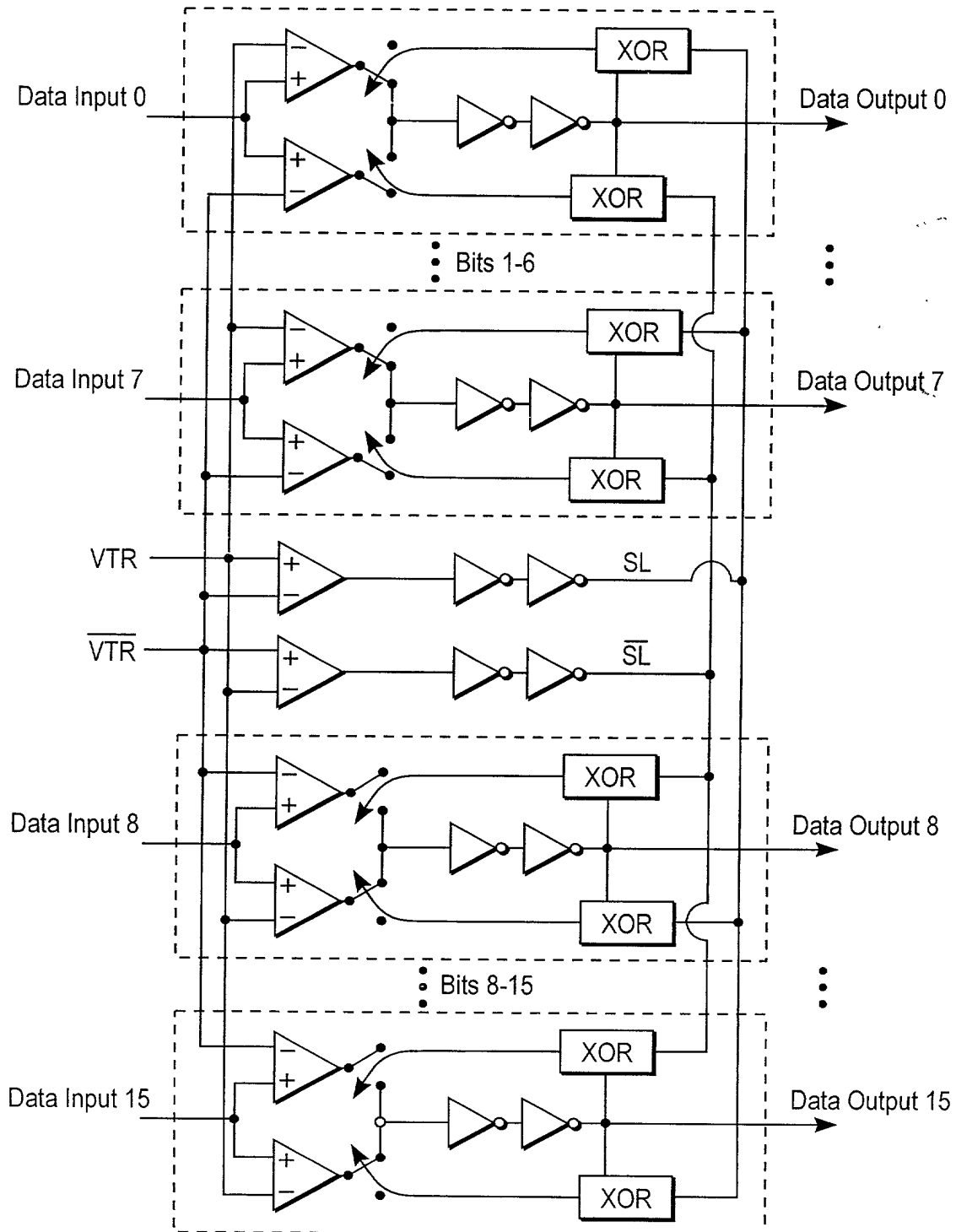


FIG. 2

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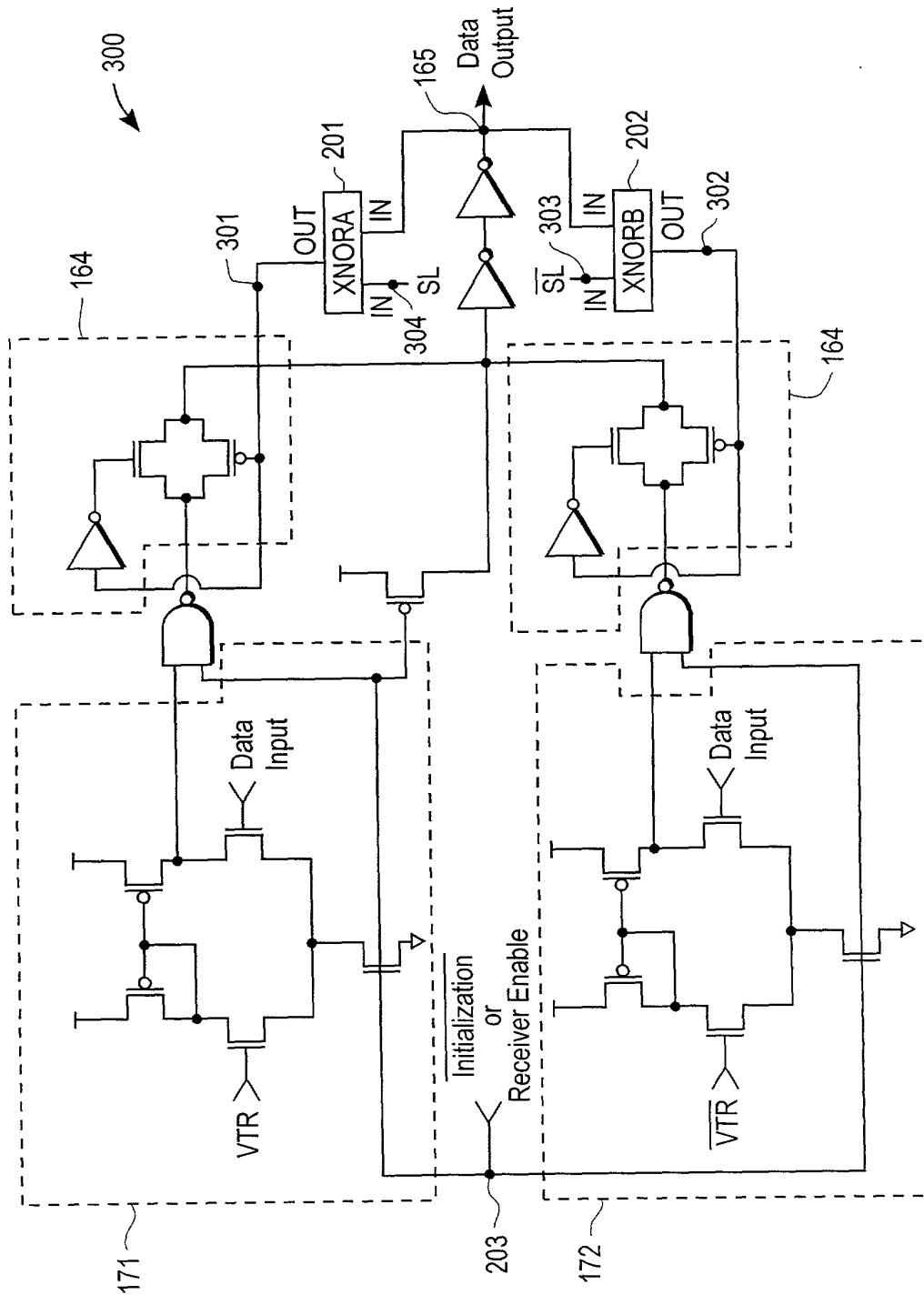


FIG. 3

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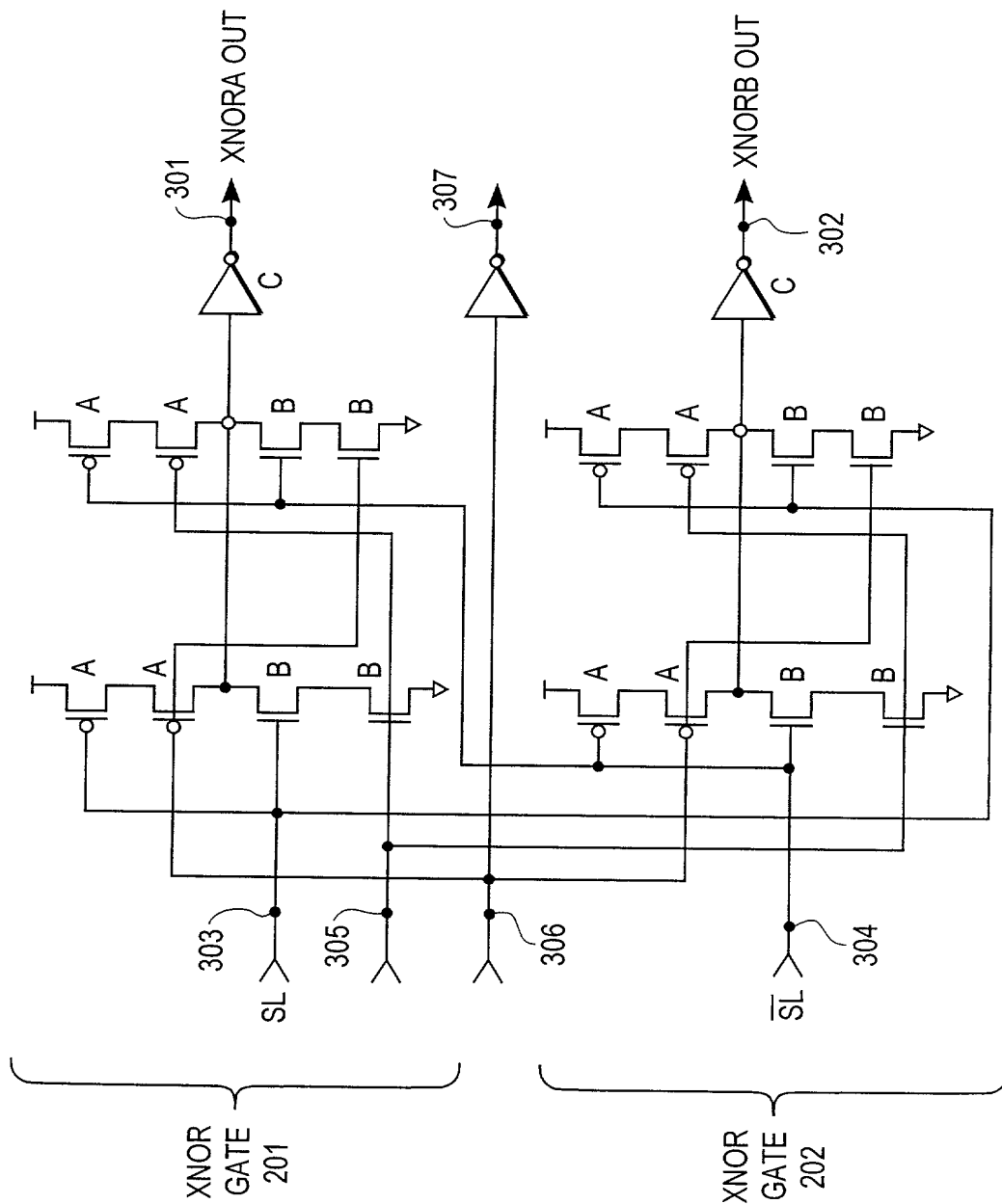


FIG. 4

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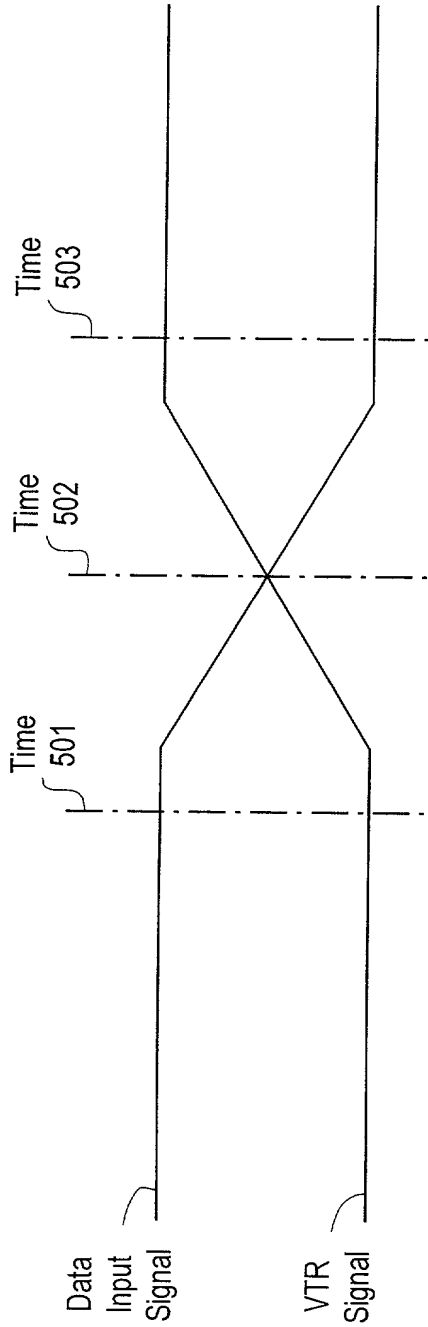


FIG. 5A

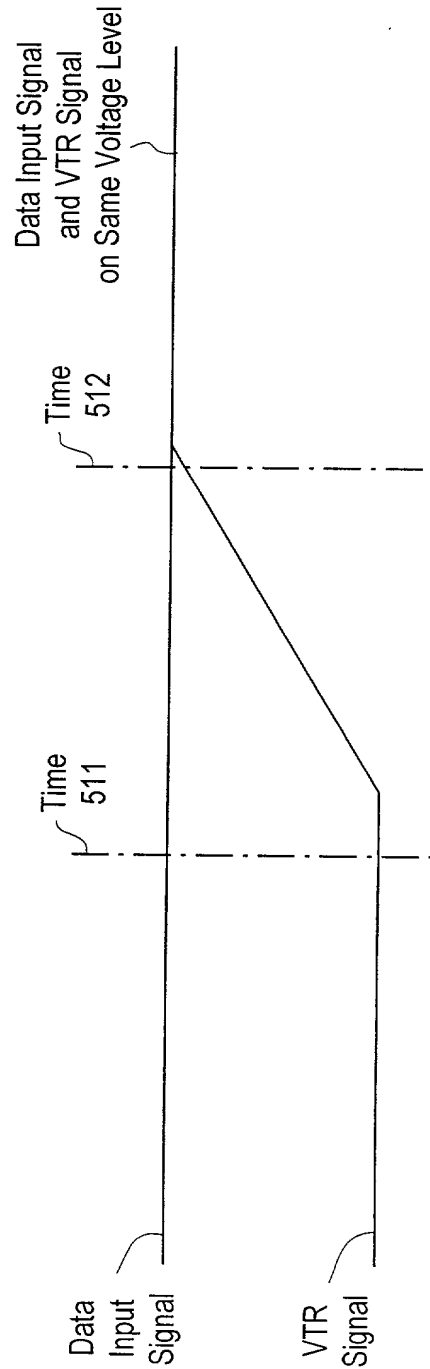
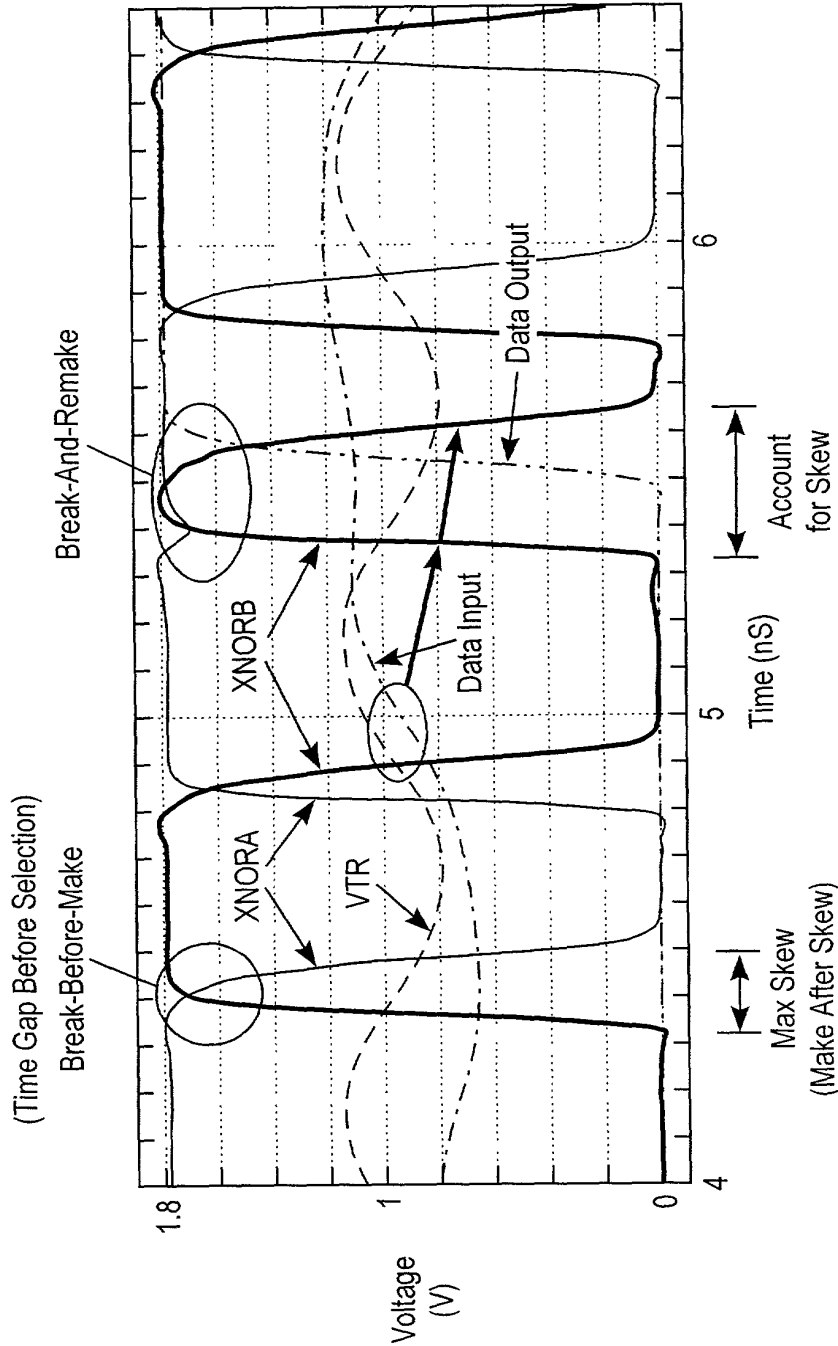


FIG. 5B

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(Replacing XOR with XNOR)

FIG. 5C

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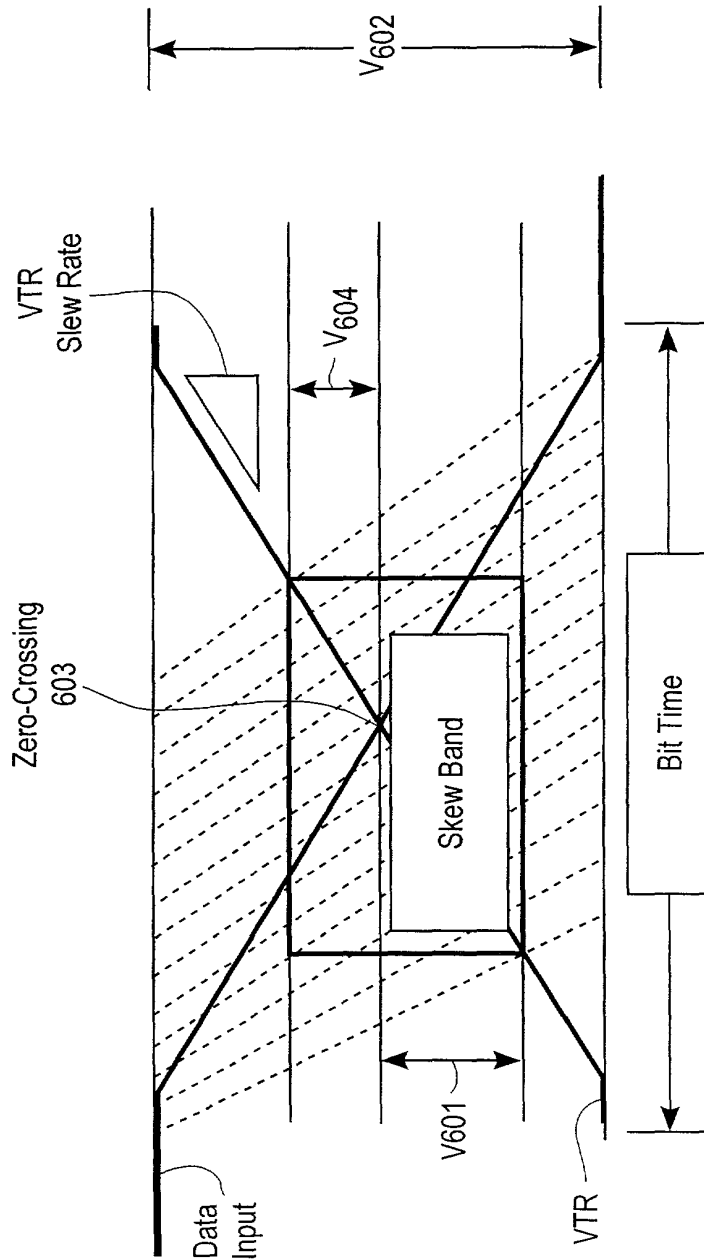


FIG. 6

[illegible]

FIG. 7A

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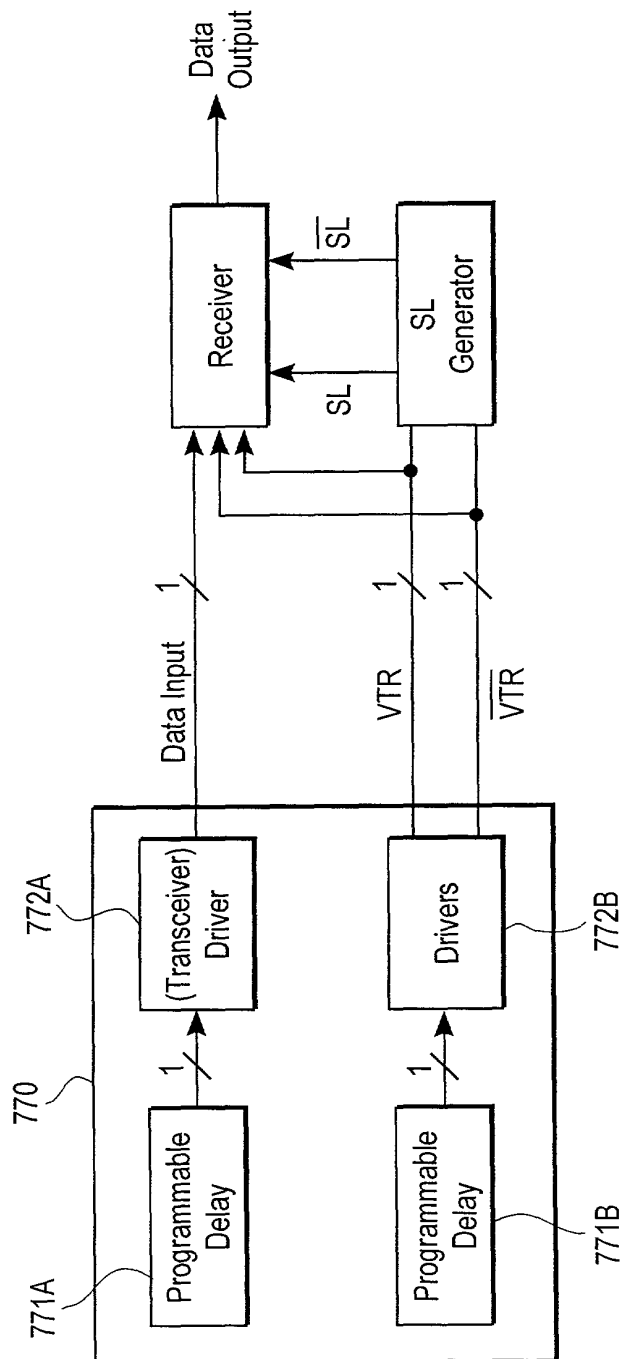
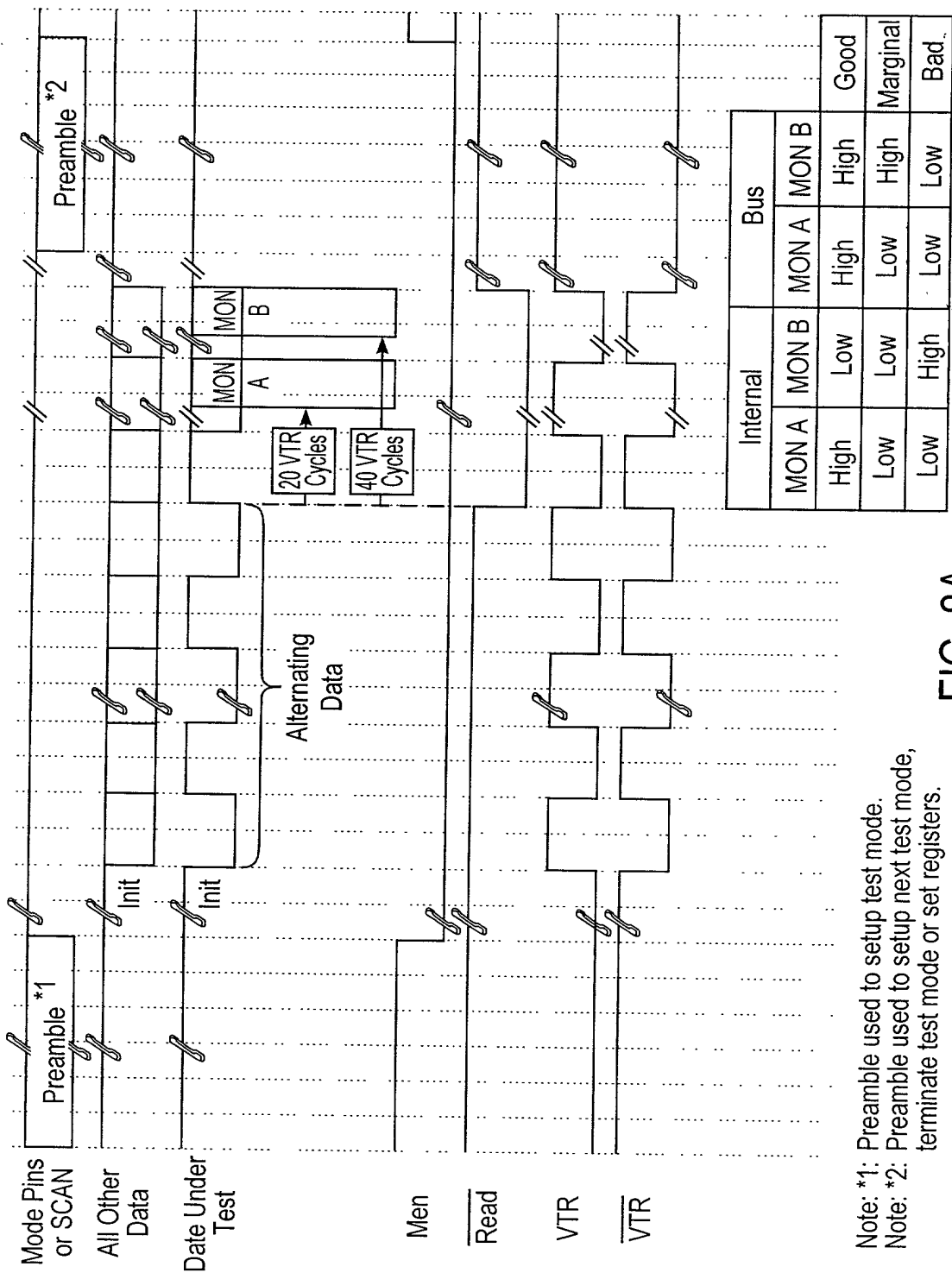


FIG. 7B

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Note: *1: Preamble used to setup test mode.
Note: *2: Preamble used to setup next test mode, terminate test mode or set registers.

FIG. 8A

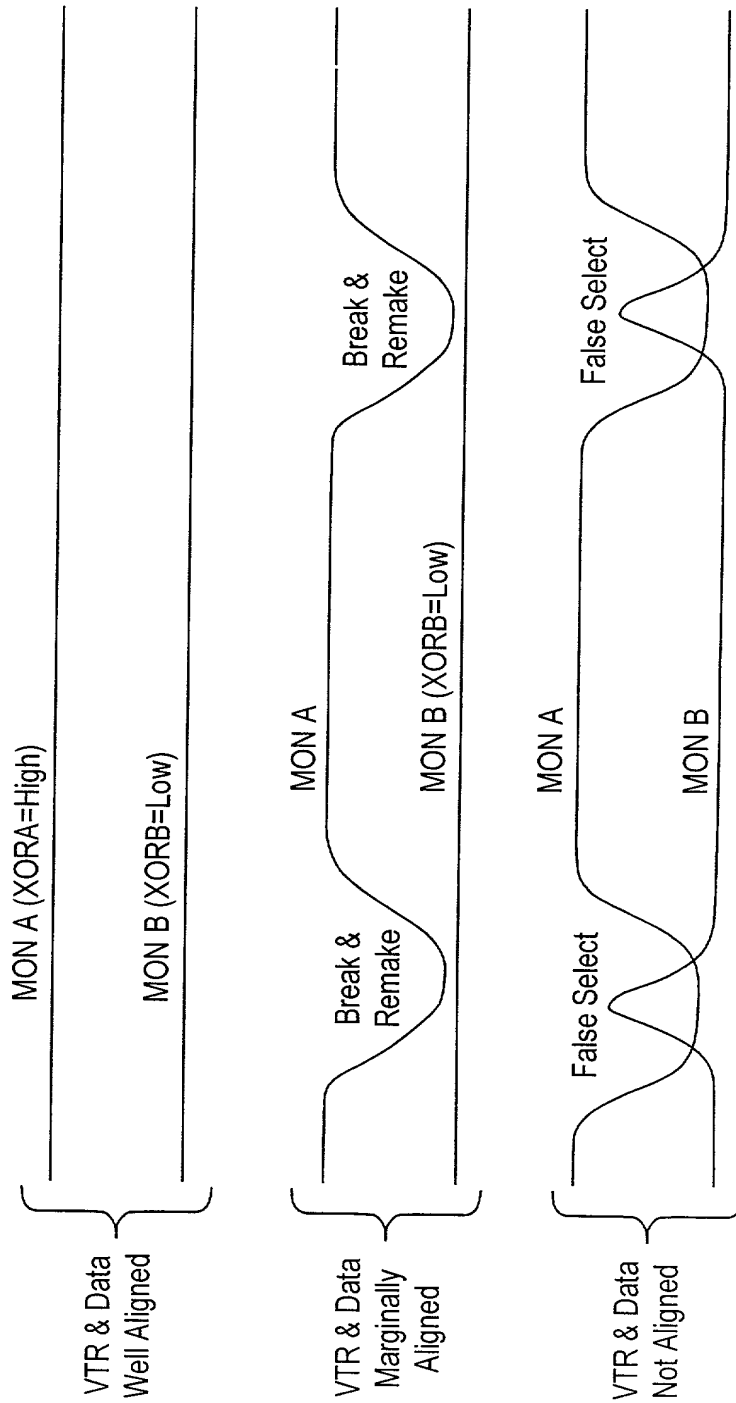


FIG. 8B

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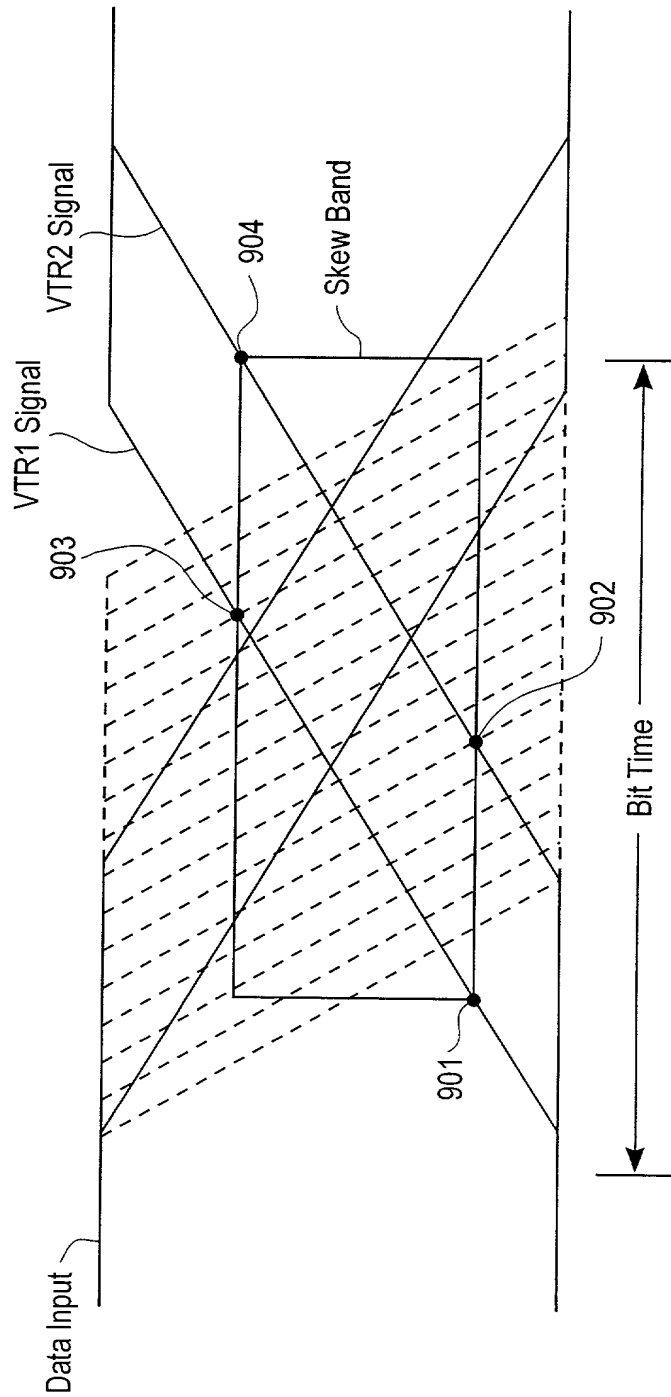


FIG. 9

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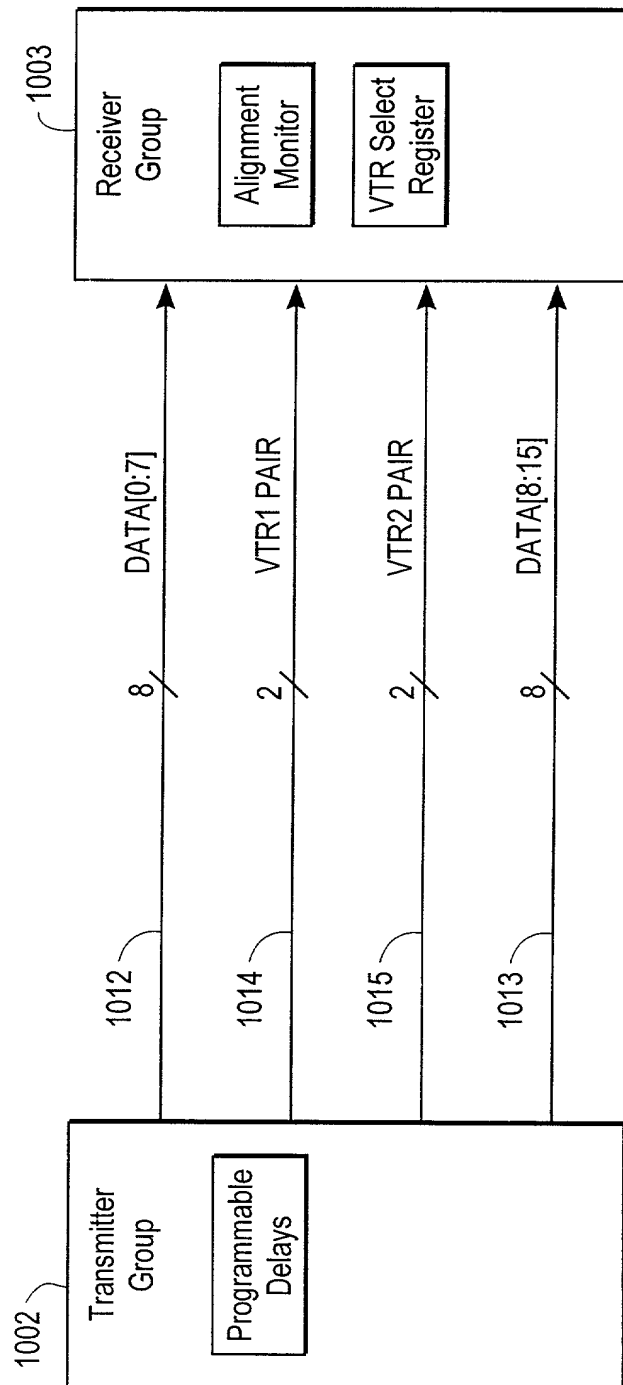


FIG. 10

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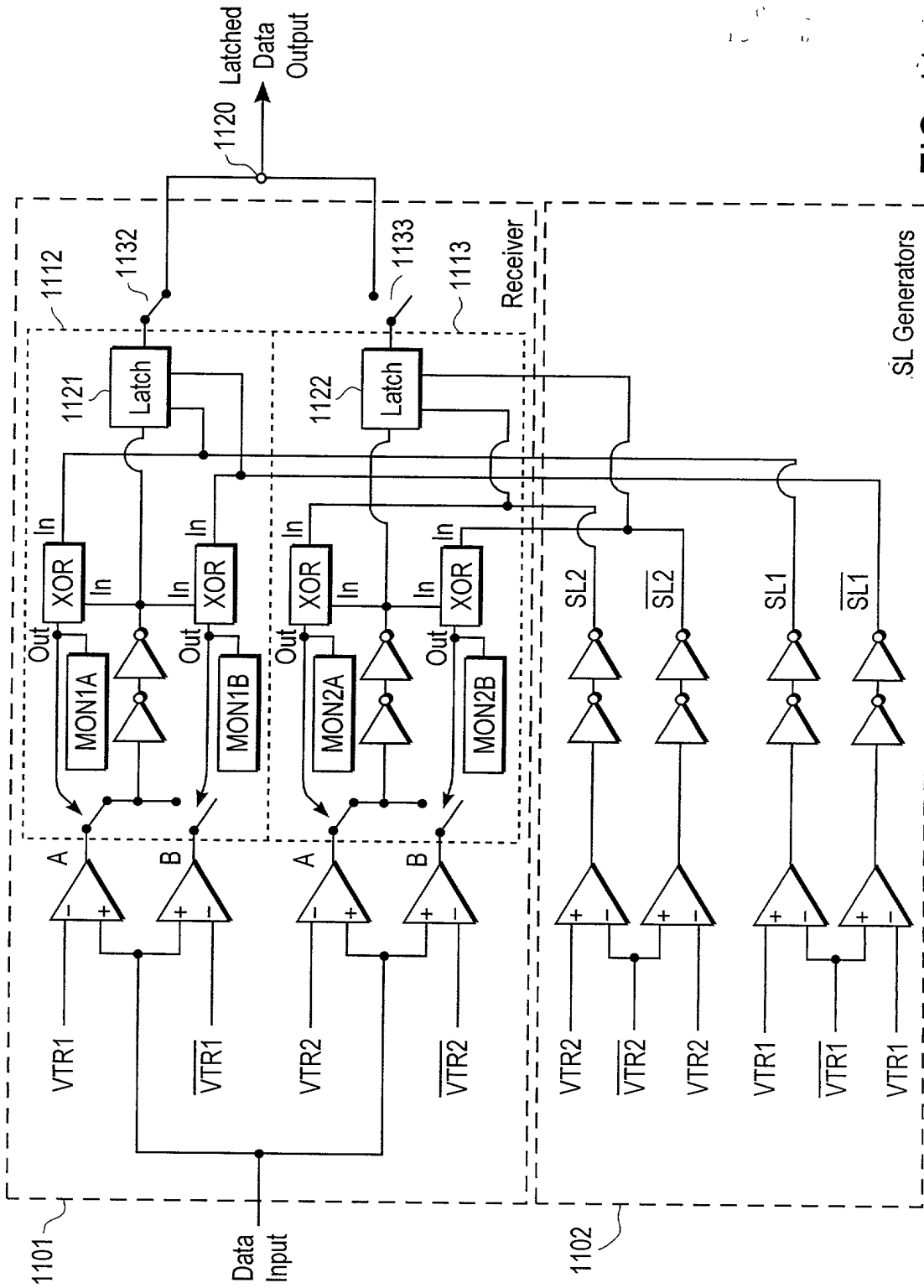


FIG. 11

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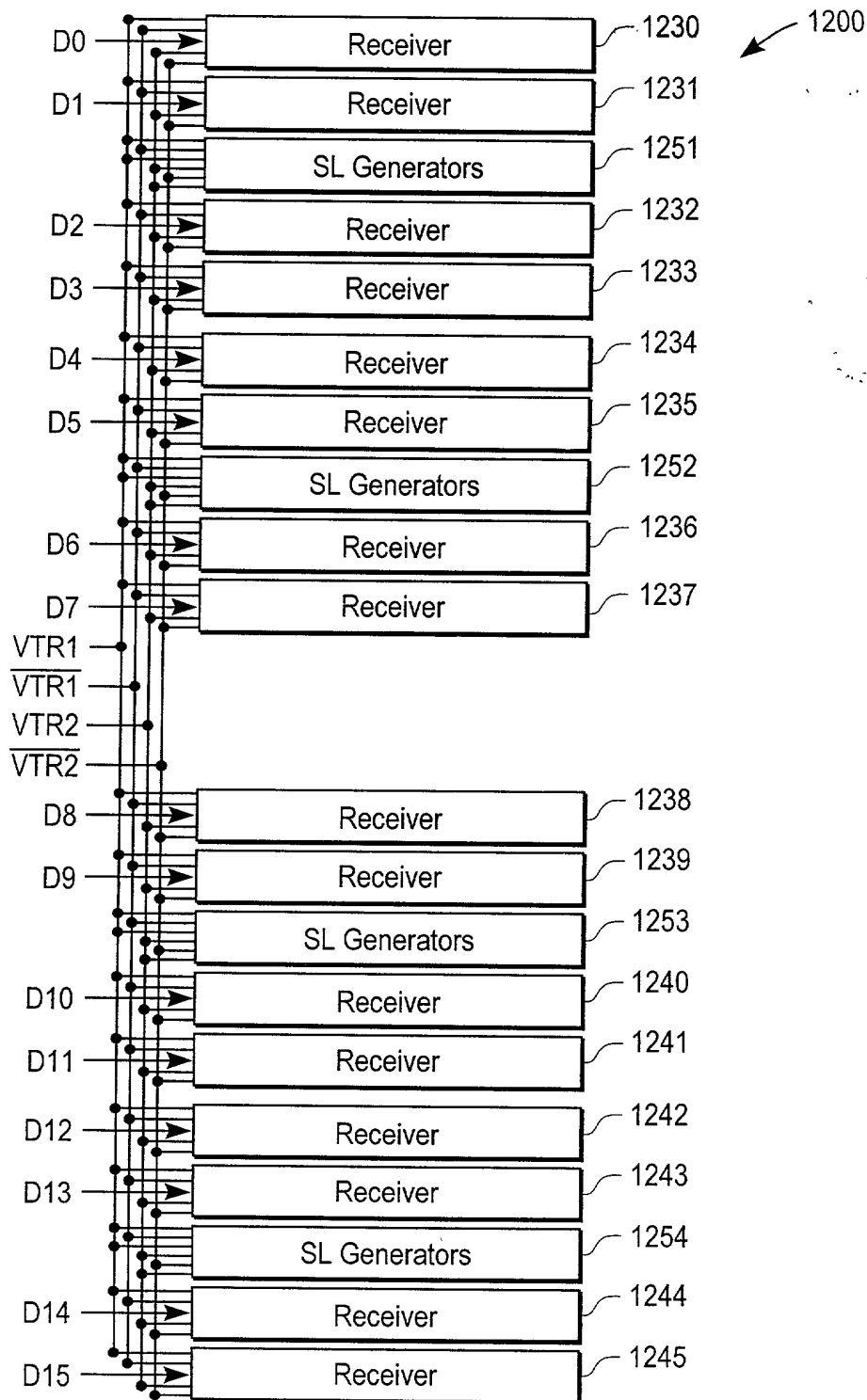


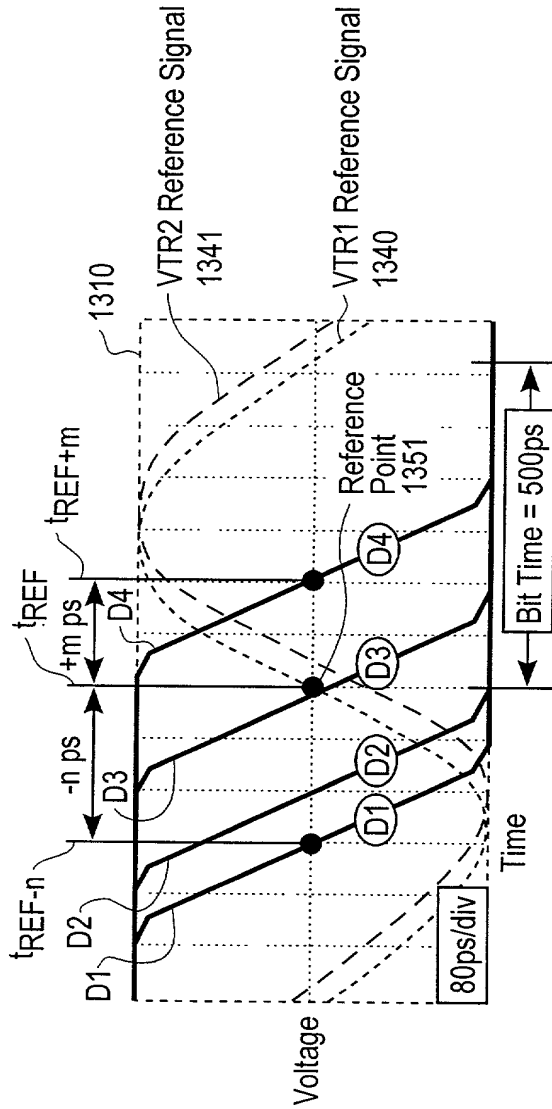
FIG. 12

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FIG. 13



Results												
	D1-80ps	D1	D1+80ps	D2-80ps	D2	D2+80ps	D3-80ps	D3	D3+80ps	D4-80ps	D4	D4+80ps
VTR2=VTR1+40ps												
VTR1 REF - 160 ps		Pass	Pass	Pass	Pass	Pass	Pass					
VTR2 REF - 160 ps		Pass	Pass	Pass	Pass	Pass	Pass					
VTR1 REF - 80 ps			Pass		Pass	Pass	Pass	Pass				
VTR2 REF - 80 ps			Pass		Pass	Pass	Pass	Pass				
VTR1 REF						Pass	Pass	Pass	Pass	Pass		
VTR2 REF						Pass	Pass	Pass	Pass	Pass		
VTR1 REF + 80 ps								Pass	Pass	Pass	Pass	
VTR2 REF + 80 ps								Pass	Pass	Pass	Pass	
VTR1 REF + 160 ps								Pass	Pass	Pass	Pass	Pass
VTR2 REF + 160 ps								Pass	Pass	Pass	Pass	Pass

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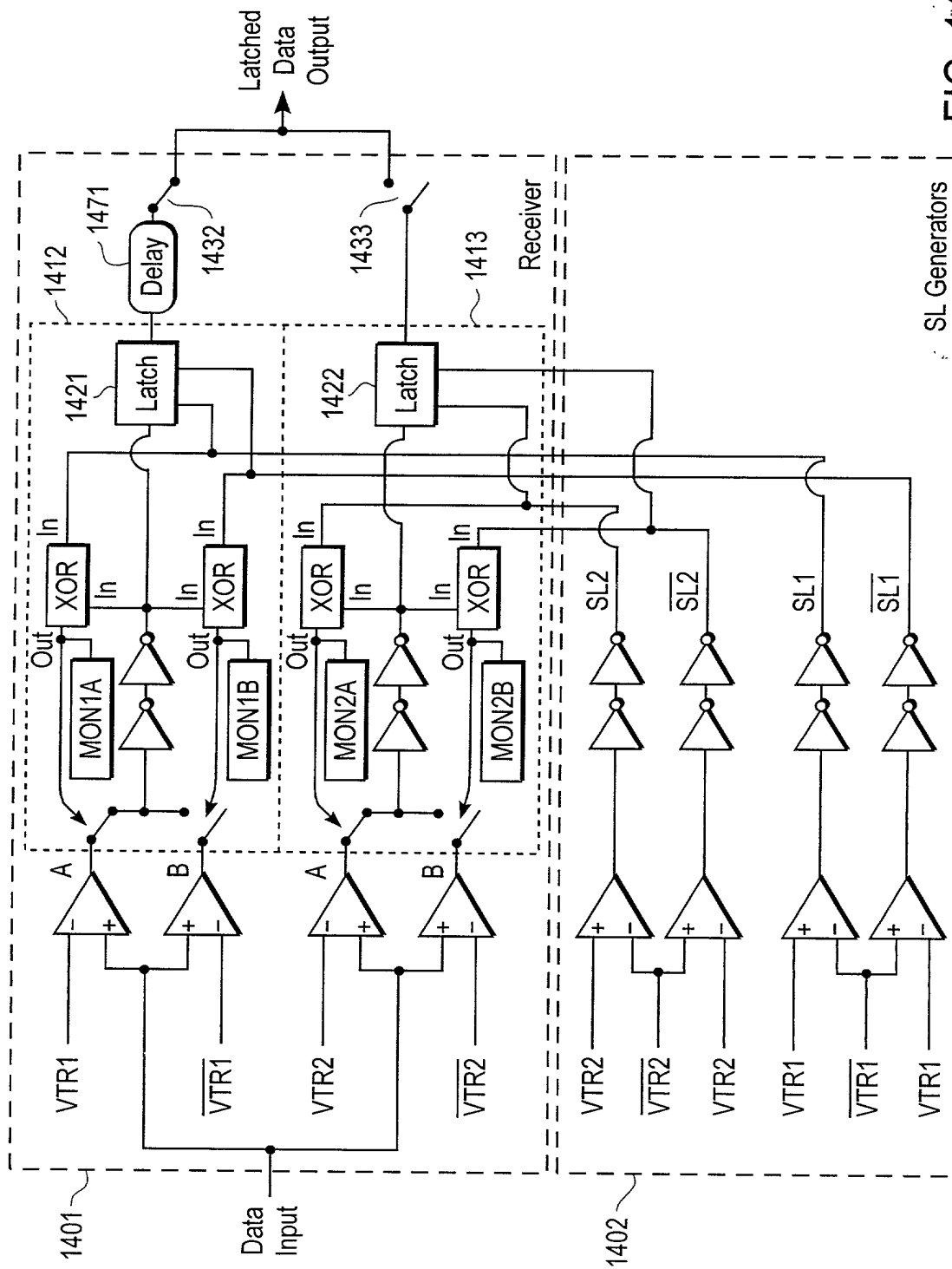


FIG. 14

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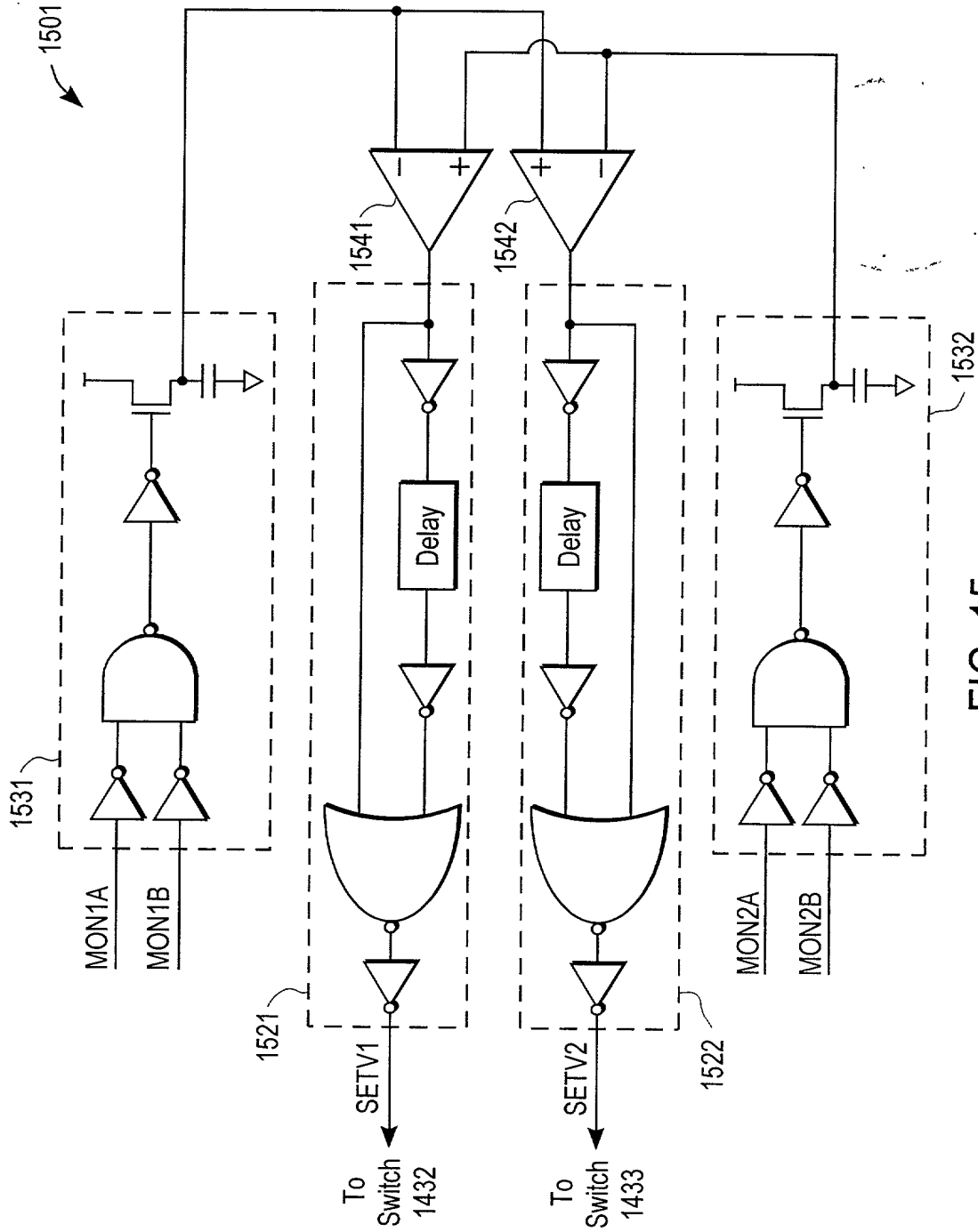


FIG. 15